Effect of sampling jitter on signal tracking in a direct sampling dual band GNSS receiver for civil aviation

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EFFECT OF SAMPLING JITTER ON SIGNAL TRACKING IN A DIRECT SAMPLING DUAL BAND GNSS RECEIVER FOR CIVIL AVIATION

This paper studies the impact of clock sampling jitter on signal tracking in a dual band L5/E5 and L1/E1 Direct Sampling GNSS receiver designed for Civil Aviation. A model of the sampling clock jitter due to thermal noise is established and related simulation results about the phase tracking error standard deviation at the output of the PLL are presented.

KEY WORDS

1. Direct Sampling   2. Dual band   3 .GNSS receiver   4. Civil Aviation
5. Sampling Jitter   6. Signal Tracking

1. INTRODUCTION

With the imminent availability of new GNSS signals dedicated to Civil Aviation, there is a growing industrial interest in the development of Dual Band L5/E5 and L1/E1 GNSS receivers dedicated to Civil Aviation usage.

Moreover, this community could take advantages of the emerging Direct Sampling technology which allows not only a valuable RF hardware simplification but also an unprecedented upgradability.

But is it possible to build a Dual Band GNSS Receiver, using Direct Sampling, compliant with the strict requirements found in Civil Aviation standards, such as Minimum Operational Performance Specification (MOPS) documents, edited by RTCA [DO-229], [DO-316], [DO-253] and EUROCAE [Galileo MOPS OS] ? In particular, it is not clear whether it could comply with the requirements of robustness against interferences, which is a specificity of Civil Aviation by its severity.

[Blais 2011] proposes an RF Front-End architecture based on the coherent Direct Sampling of both bands. This paper exhibits filters which are necessary to meet requirements on interferences when considering aliasing and also assesses the characteristics of the digitization process by calculating the required sampling frequency and the number of bits of the ADC.

The present article goes further on the evaluation of the Direct Sampling solution for Civil Aviation receivers by studying the sampling jitter effect on signal tracking.

In a first part we review the architecture exposed in [Blais 2011] and we complete it by an alternative one. Then the phenomenon of sampling jitter is exposed in a second part. And finally a third part presents some simulation results about the influence of sampling jitter on signal tracking.

2. DUAL BAND GNSS RECEIVER ARCHITECTURES FOR CIVIL AVIATION

[Blais 2011] proposes to set the useful L5/E5 and L1/E1 bands to respectively $[f_{min5}, f_{max5}]$ = [1166.45, 1211.14] MHz and $[f_{min1}, f_{max1}]$ = [1565.42, 1585.42] MHz as they are considered as the most sensitive part of the spectrum in the standards [DO-229], [DO-316], [DO-253] and [Galileo MOPS OS]. We will do the same here.

If Direct Sampling is to be used in a Dual Band GNSS receiver for Civil Aviation, [Blais 2011] also proposes to go as far as possible into hardware simplification by removing the need of AGC. Again we will do the same here.

Then two architectures can be proposed. The first one, which immediately follows, is already presented in [Blais 2011] and is shown on Figure 1. The second one is an evolution.

2.1. COHERENT SAMPLING ARCHITECTURE

From a Signal Processing point of view this solution has the advantage of sampling coherently both bands.
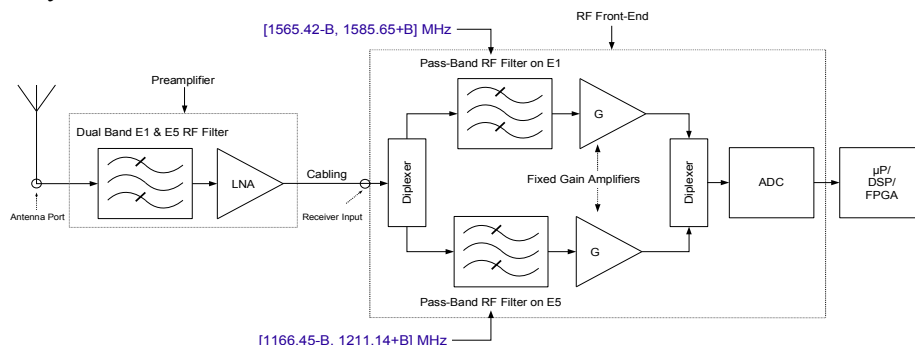

Figure 1: Direct Coherent Sampling Architecture

This property may be used by the following navigation processes but induces three dimensioning constraints :

- From the antenna port to the input of the ADC, the RF paths parameters (in particular phase and group delays) must be measured for each band in order to equalize both channels after digitization.
- The minimum sampling frequency to be used is higher than if each band is sampled separately. From [Blais 2011], figure 2 shows the minimum sampling frequency F_s as a function of the transition bandwidth B of the Pass-Band RF filters. F_s is defined as the lowest sampling frequency for which $[f_{min5}-B, f_{max5}+B]$ and $[f_{min1}-B, f_{max1}+B]$ do not overlap by aliasing. The bound is F_s = 151 MHz, for a 0 MHz transition bandwidth. This result is to be compared to the minimum sampling frequencies involved in the next proposed architecture.
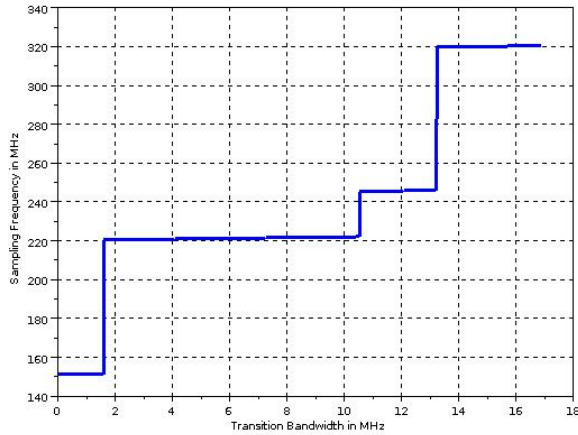- The two bands need to be separated and decimated after digitization.

Figure 2: Minimum Sampling Frequency for Coherent Sampling, as a function of the transition bandwidth

2.2. SEPARATE SAMPLING ARCHITECTURE

If there is no need of coherency between both bands in following navigation processes, the L5/E5 band and the L1/E1 band can be sampled separately, relaxing the previously mentioned constraints. This solution is represented on Figure 3.
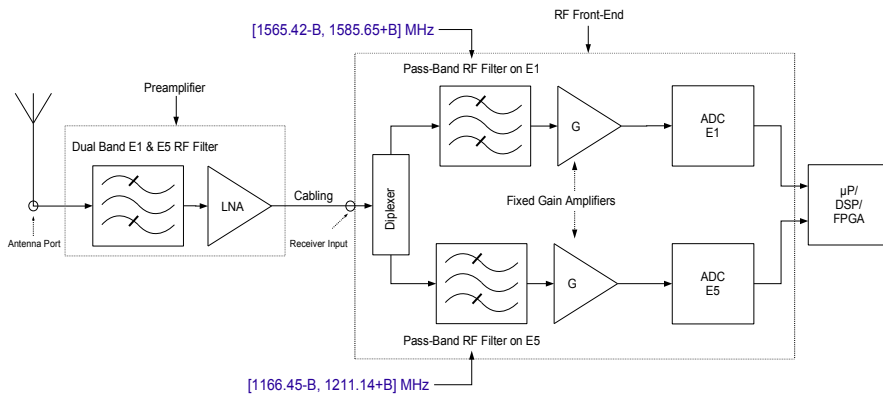

Figure 3: Direct Separate Sampling Architecture

As each band can be sampled without taking care of aliasing on the other one, the minimum sampling frequency for each band is much lower than the unique minimum sampling frequency required for coherent sampling. This appears clearly on Figure 4 which again represents the minimum sampling frequency, but for each band this time, as a function of the transition bandwidth of the Pass-Band RF filters.

The bounds are $F_s = 89.714$ MHz and $F_s = 40.137$ MHz for respectively the L5/E5 band and the L1/E1 band, for a 0 MHz transition bandwidth.
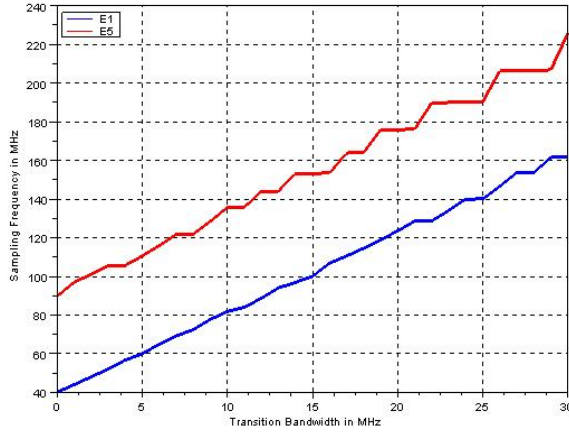
Figure 4: Minimum Sampling Frequency for Separate Sampling, as a function of the transition bandwidth

For the sake of completeness, it should be noted that there are two distinct sample flows to be processed in this architecture instead of a single one previously.

3. SAMPLING JITTER MODEL

In an Analog to Digital Converter (ADC), the sampling operation is triggered by the level crossing of a threshold by a clock signal, as represented on Figure 5. Let us denote T_s the sampling period and $\{t_n=nT_s, n\in\mathbb{Z}\}$ the set of ideal sampling instants.
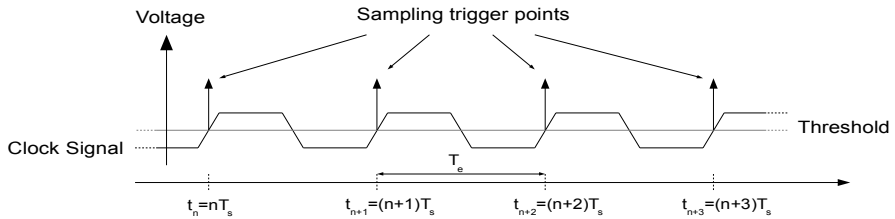

Figure 5: Ideal Sampling Instants

Due to noises, the clock signal does not cross the threshold at exactly equally spaced $\{t_n\}$ but at some $\{t_n'\}$, thus introducing a bias in the sampling operation : this phenomenon is called sampling jitter.

Sampling jitter must be taken into account when designing a Direct Sampling Receiver because the sampled frequencies are, by definition, much higher than in classical architectures where digitization occurs at relatively low Intermediate Frequencies (IF). It means that, in Direct Sampling receivers, the slope of the input signal is proportionally so high that a small deviation of the sampling instant can induce a large error in amplitude as drawn on Figure 6.
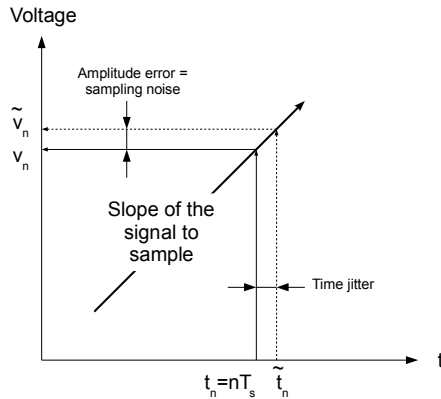
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Figure 6: Time Jitter ⇒ Amplitude Error

Depending on the type of noise, a distinction is made on the type of the resulting jitter.

3.1. APERTURE JITTER

This jitter is due to the noise which adds to the amplitude of the clock, such as the thermal noise of the ADC.

The Figure 7 shows how this amplitude noise contribution moves the sampling instant away from its ideal position, because of the slope of the clock.
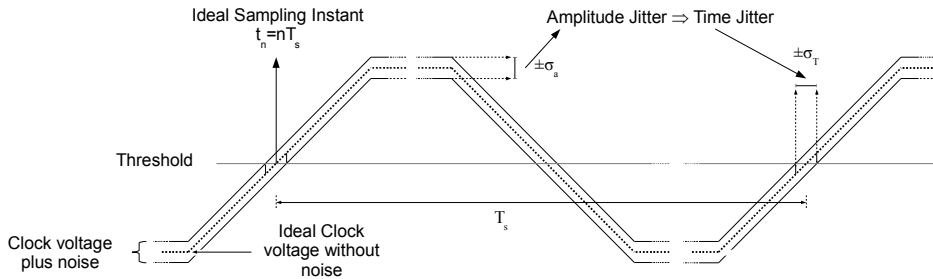
Figure 7: Aperture Jitter

This type of jitter has been extensively studied in general as in [Shinagawa 1990] or [Kobayashi 2002] for example, and in the particular case of GNSS receivers in [Dempster 2004], [Dempster 2005] and [Dempster] so we won't develop more on this topic in this article.

3.2. CLOCK JITTER

The clock, which periodically triggers the ADC, is built on an underlying oscillator which is also subject to electronic noises.

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Let $x_s(t)$ be the noiseless ideal periodic signal expected at the output of this oscillator. For example a sinusoidal waveform with fundamental frequency F_S : $x_s(t)=sin(2\pi F_s t)$

As $x_s(t)$ is periodic, we can define its phase $\Psi(t)=2\pi F_s t$.

But instead of this ideal model, the output waveform of a real oscillator should be modeled, as proposed in [Lee 2001], by :

$$x(s(t))=x_s(s(t))+y(s(t))$$

where :

- y(.) represents the additive distortion in the amplitude domain,
- s(t) = t + j(t) models the distortion in the time domain, with j(t) defined hereafter.

Both perturbations mainly find their origin in the thermal noise and in the flicker noise which are inherently present in any electronic device.

From now on we will focus on the time perturbation j(t), as y(.) can be taken into account in the aperture jitter presented previously.

As we are working with a periodic signal, the jitter term j(t) can be expressed in a more expressive way as a phase deviation :

$$j(t)=\frac{T_s}{2\pi}\phi(t)$$

which gives $x_s(s(t))=sin(2\pi F_s t+\phi(t))$ in our example.

In the rest of this paper, we will only deal with the effect of thermal white noise. The effect of flicker noise on signal tracking performances should be studied later.

Over the time interval [t_1, t_2], the phase difference $\phi(t_2)-\phi(t_1)$ results from the action of numerous independent and identically distributed noise contributors, as the Brownian motion of electrons, and thus can be modeled, according to the Central Limit theorem, as a Gaussian random variable.

What is more, $\forall$ t_1, t_2, t_3 and t_4 such that $0 \le t_1 \le t_2 \le t_3 \le t_4$, one can make the assumption that $\phi(t_2)-\phi(t_1)$ and $\phi(t_4)-\phi(t_3)$ are independent random variables.

Thus, by extension, the phase deviation $\phi(t)$ can then be modeled as a Brownian motion or non-stationary Wiener process, and described by the following integral :

$$\phi(t)=\frac{2\pi}{T_s}\sqrt{c}\int_0^t w(u)du$$

where $w\sim N(0,1)$ and w(t) and w(t+τ) are independent random variables $\forall \tau \ne 0$.

It must be noted that by nature $\phi(t)$ is an unbounded process.

The constant c is the variance of j(t), in s, by unit of time. It is a characteristic of the oscillator which can be measured from the oscillator phase spectrum as proposed in [Zanchi 2003] or [Drakhlis, 2001]. For modern integrated oscillator c is in [10^{-19}, 10^{-21}] s while TCXO and OCXO can reach 10^{-25} s as suggested in [Löhning 2007].

If such a noisy clock is used to trigger the ADC by threshold crossing (zero for simplicity), we can write that

- crossing N°n will occur at time

$$2\pi F_s \tilde{t}_n = 2\pi F_s(n T_s) + \phi(\tilde{t}_n) = 2\pi n$$

- and the next one at time

$$2\pi F_s \tilde{t}_{n+1} = 2\pi F_s((n+1)T_s) + \phi(\tilde{t}_{n+1}) = 2\pi(n+1)$$

That is :

$$\tilde{t}_{n+1} = \tilde{t}_n + T_s + \frac{\phi(\tilde{t}_{n+1}) - \phi(\tilde{t}_n)}{2\pi F_s} = \tilde{t}_n + T_s + \sqrt{c} \int_{\tilde{t}_n}^{\tilde{t}_{n+1}} w(u)\, du \quad .$$

If the time jitter is small in comparison to the period T_s, we can then approximate this integral with fluctuating limits by an integral with constant limits :

$$\int_{\tilde{t}_n}^{\tilde{t}_{n+1}} w(u)\, du \approx \int_0^{T_s} w(u)\, du \sim N(0, T_s)$$

as $\phi(t)$ is a Wiener process, that is a process with stationary increments.

Thus we can simulate the jittered sampling instants by using the iterative formula :

$$\tilde{t}_{n+1} = \tilde{t}_n + T_s + \Delta T_s, \quad \Delta T_s \sim N(0, c T_s) \quad \text{with} \quad \tilde{t}_0 = 0 \quad .$$

4. EFFECT OF SAMPLING CLOCK JITTER ON SIGNAL TRACKING

To study the effect of sampling clock jitter on GNSS signal tracking, two software modules were developed :

- a L1 signal generator, which produces a useful navigation signal disturbed by a white noise at a given C/N0 ratio. This composite signal is generated directly at the jittered sampling instants, according to the model presented hereinbefore, with a customizable constant c.
- a software receiver, dedicated to L1 signal processing in a first time. However no filter was implemented so as to directly observe the sampling clock jitter effect. Regarding the tracking function, after a transition period where a FLL is used to finish acquisition and then disconnected, the measures are obtained using a classical dual DLL-PLL architecture. The PLL model is drawn on Figure 8.

We focused on the phase tracking error standard deviation, as the phase, θ[n] on the diagram 8, is the most sensitive parameter in signal tracking. Knowing the instantaneous phase of the signal produced by our generator, we were able to calculate the phase tracking error at any time and hence its statistics.
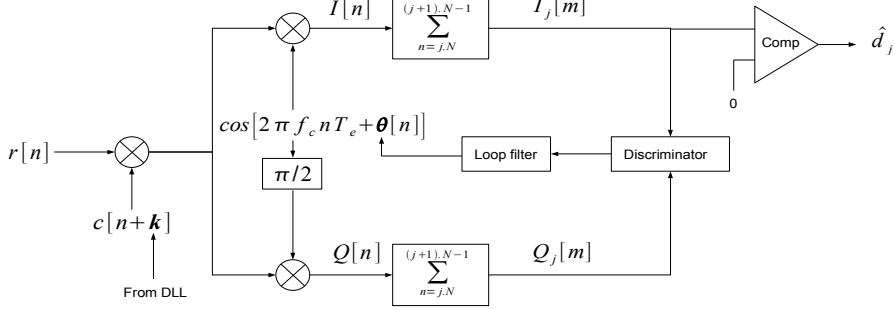
Figure 8: PLL Model

4.1. SIGNAL GENERATOR – SOFTWARE RECEIVER VALIDATION

A dry-run was done without jitter to validate this duo. The phase tracking error standard deviation at the output of the PLL shows good accordance to the theoretical bound found in [Holmes 1990] as we can see on Figure 9.
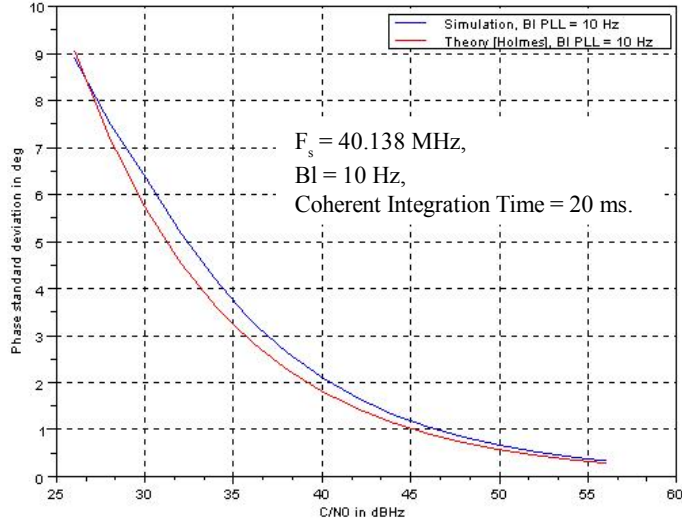

F_s = 40.138 MHz,
Bl = 10 Hz,
Coherent Integration Time = 20 ms.

Figure 9: Simulation results vs Theory [Holmes 1990]

Bl denotes the noise equivalent bandwidth of the PLL and of the DLL.

4.2. PHASE TRACKING ERROR STANDARD DEVIATION VS C/N0 AND CONSTANT C

Figure 10 shows (black) plots for c = {10^{-25}, 2.10^{-25}, 10^{-24}, 2.10^{-24}, 10^{-23}, 2.10^{-23}} s.
Figure 11 is a close-up view for c = {10^{-25}, 2.10^{-25}, 10^{-24}, 2.10^{-24}} s.
The blue plot corresponds to the theoretical bound found in [Holmes 1990].

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We can clearly distinguish two regions.

The first one, for strong C/N0 ratios, shows that an increase of c has an exponential effect on the phase tracking error standard deviation : at C/N0 = 56 dBHz, a multiplication by 2 of $c = 10^{-25}$ s provokes a degradation of around 0.25° of the phase tracking error whereas a multiplication by 2 of $c = 10^{-24}$ s provokes a degradation of nearly 1°.
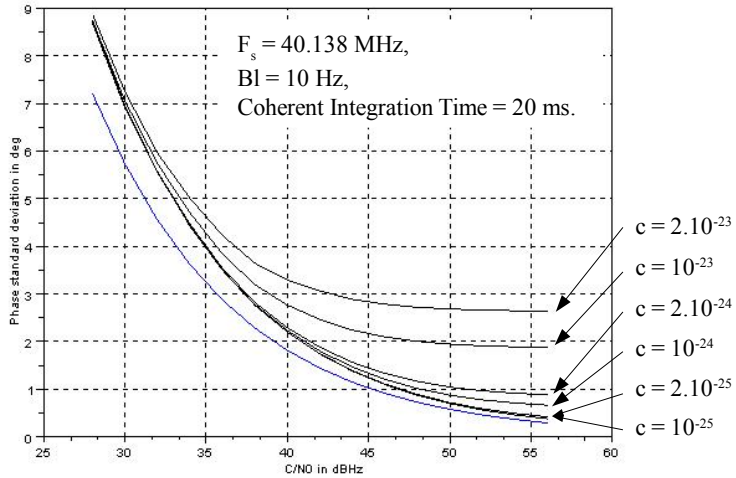

Figure 10: Phase Tracking Error Standard Deviation vs C/N0 and Constant c

The second one is for C/N0 ratios lower than 30 dBHz : whatever the value of c, all the plots join. The sampling clock jitter provokes a degradation of the phase tracking error standard deviation which is equivalent to a loss of around 1.6 dB in C/N0.
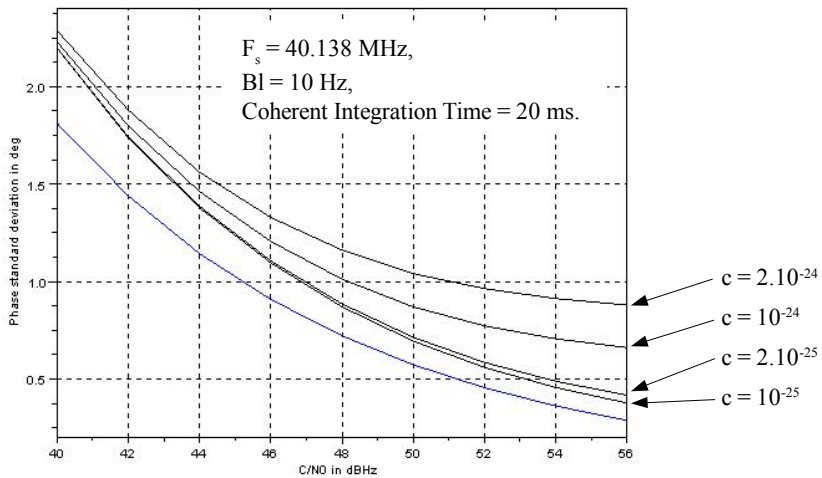

Figure 11: Phase Tracking Error Standard Deviation vs C/N0 and Constant c, a close-up view.

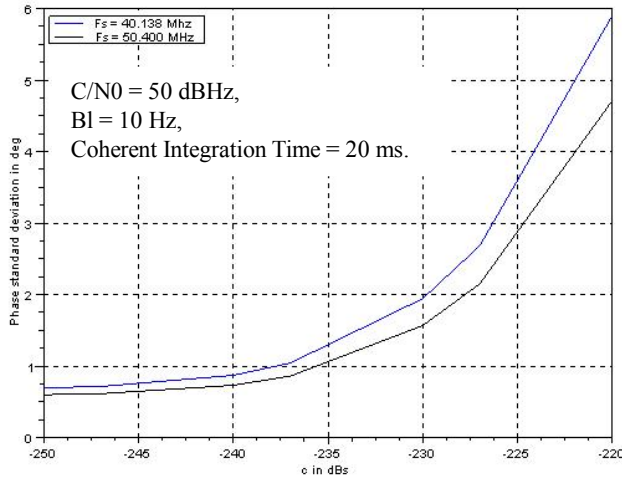## 4.3. PHASE TRACKING ERROR STANDARD DEVIATION VS SAMPLING FREQUENCY F_S AND CONSTANT C

Figure 12: Phase Tracking Error Standard Deviation vs F_s and Constant c

Figure 12 shows clearly that the higher the sampling frequency the lower the clock sampling jitter effect.

This is due to the fact that between two sampling instants jitter does have less time to accumulate when the sampling frequency is higher.

5. CONCLUSIONS

In summary we have reviewed an architecture for a Direct Sampling GNSS receiver designed for the E5/L5 and E1/L1 bands and intended for Civil Aviation usage, and then proposed a new one. Due to the high input frequencies involved in such architectures, we found it necessary to assess the tracking performances of such receivers facing the sampling clock jitter problem. So a model of sampling clock jitter was studied and implemented in a signal generator, coupled with a software receiver to calculate the statistics of the phase tracking error induced at the output of the PLL. Some results were presented to conclude this paper.

Our future work shall focus on the effect of sampling clock jitter due to flicker noise.

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